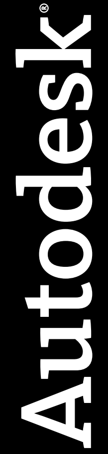
Autodesk® Moldflow® Insight 2012

AMI Wire Sweep Analysis



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Wire sweep analysis

1

A wire sweep analysis is used to predict the deformation of the bonding wires within the cavity.

A wire sweep analysis is run as part of the microchip encapsulation molding process. It is used to calculate the deformation of the bonding wires (connecting the chip to the leadframe) that occurs during encapsulation. This calculation enables you to improve the mold design and process conditions to prevent wire-sweep from occurring during encapsulation. The wire deformation can be calculated either internally in Autodesk Moldflow Insight using the Warp module or externally using Abaqus.

3D Microchip Encapsulation also supports a Wire Sweep Detail analysis, which accounts for the effects of the wires on the fluid flow as well as the effects of the fluid on the wires. The 3D chip cavity model must include the wire cavities as well as the wires themselves. The Wire Sweep Detail analysis takes more time to complete compared to the regular Wire Sweep analysis, but the calculation of deformation can be more accurate.

Wire sweep analysis

Wire Sweep analysis is used to analyze the deformation of bonding wires that connect the chip to the leadframe during the microchip encapsulation process.

Running a wire sweep analysis

Ensure you have specified microchip encapsulation as your molding process.

1. Click **Home tab > Molding Process Setup panel > Analysis Sequence**.
2. In the **Select Analysis Sequence** dialog, select **Fill+Pack+Wire Sweep** or **Fill+Pack+Wire Sweep Detail** and then click **OK**.
3. If these options are not visible, click **More** to show more analysis options.
4. If necessary, double-click from the Study Tasks pane to change the Material properties.
5. If necessary, double-click from the Study Tasks pane to edit the Process Settings properties.
6. Double-click **Start Analysis!** from the **Study Tasks** pane, or **Home tab > Analysis panel > Start Analysis**.

NOTE: Click **Home tab > Analysis panel > Job Manager > Abort Job** to abort the analysis.

Modeling for wire sweep detail analysis (3D)

2

Wire Sweep analysis is used to analyze the deformation of bonding wires that connect the chip to the leadframe during the microchip encapsulation process.

3D Microchip Encapsulation includes a Wire Sweep Detail analysis that accounts not only for the effect of fluid flow on the wires but also for the effect of the wires on the fluid flow. To perform a Wire Sweep Detail analysis, the 3D model of the chip cavity must include the wire cavities, which are modeled as void regions in the 3D mesh.

Table 1: Wire Sweep Detail analysis compared to Wire Sweep analysis

Wire Sweep Detail	Wire Sweep
Wire cavity regions are included (modeled as voids) in the 3D model of the chip cavity for Fill+Pack analysis.	Wire cavity regions are not included in the 3D model of the chip cavity for Fill+Pack analysis.
Accounts for the effect of wires on fluid flow in the Fill+Pack analysis.	The effect of wires on fluid flow is not considered in the Fill+Pack analysis.
Wires are modeled as 1D beam elements with wire properties, located within the void regions in the chip cavity mesh.	Wires are modeled as 1D beam elements with wire properties.

Special modeling considerations for Wire Sweep Detail analysis

For a Wire Sweep Detail analysis, model each wire cavity as a void region in the 3D model of the chip cavity. This is because no encapsulant polymer will fill the area occupied by the wire. In this way, the Fill+Pack analysis can account for the effect of the wires on the fluid flow as the encapsulant fills around the wire cavity regions.

The mesh near the wire cavities needs to be refined to get a good analysis result. Because a wire is very long compared to its diameter, to mesh around the wire cavities following typical aspect ratio guidelines requires too many elements. To use a reasonable number of elements for Wire Sweep Detail analysis, the chip cavity mesh will include high-aspect-ratio elements near the wire cavities.

Each wire should be meshed with 1D beam elements with wire properties assigned.

The wire elements should be located within the voids that represent the wire cavities in the 3D chip cavity mesh.